September 1995
Edition 4.0a

FUJITSU

DATA SHEET

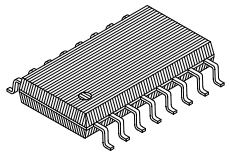
MB1507

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 2.0GH$_Z$ PRESCALER

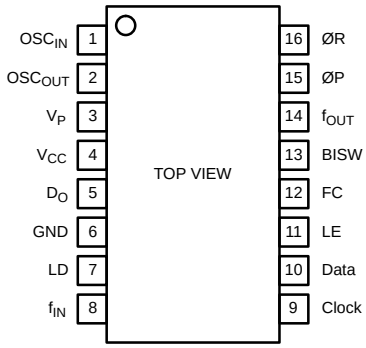
The Fujitsu MB1507 is a single chip serial input PLL frequency synthesizer designed for Broadcast Satelite tuner and cellular telephone applications.
It contains a 2.0 GH$_Z$ dual modulus prescaler which enables pulse swallow function, and an analog switch to speed up lock up time.
It operates supply voltage of 5.0V typ. and dissipates 18mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: $f_{IN\ MAX}$=2.0GH$_Z$ ($P_{IN\ MIN}$=–4dBm)
- Pulse swallow function: 128/129 or 256/257
- Low supply current: I_{CC}=18mA typ.
- Serial input 19-bit programmable divider consisting of:
  - Binary 8-bit swallow counter: 0 to 255
  - Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 8 to 16383
  - 1-bit switch counter (SW) Sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic Flat Package (Suffix: –PF)



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



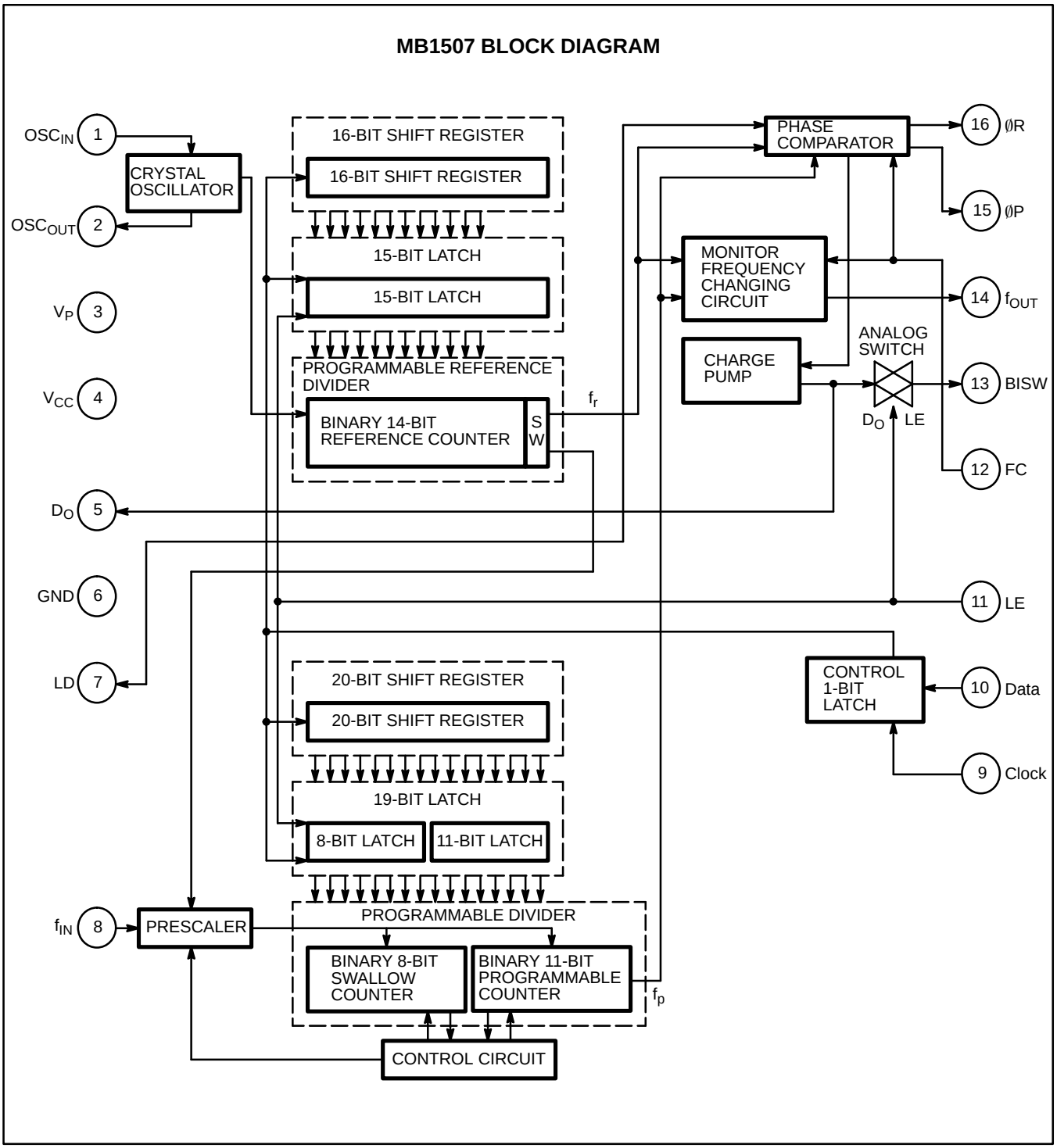
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 8.0	V
Output Current	I_{OUT}	+10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1507 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	–	Power supply input for charge pump and analog switch.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
6	GND	–	Ground.
7	LD	O	Phase comparator output. Normally the output level is high level. While the phase difference of f_r and f_p exists, the output becomes low level.
8	f_{IN}	I	Prescaler input. The connection with VCO should be AC connection.
9	Clock	I	Clock input for 20-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 19-bit latch.
11	LE	I	Load enable input (with pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phase select input of phase comparator (with pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC pin input signal controls f_{out} pin (test pin) output level, f_r or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump output.
14	f_{OUT}	O	Monitor pin of phase comparator input. f_{out} pin outputs programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
15 16	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ∅P pin is N-channel open drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15–bit programmable reference divider and 19–bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15–bit latch.
Control data "L" data is transferred into 19–bit latch.

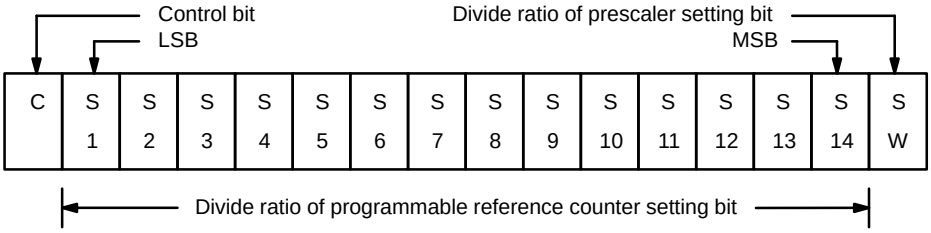
THE DIVIDE RATIO SETTING

$f_{VCO}=[(MxN)+A]xf_{OSC}\div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
M: Preset modulus of external dual modulus prescaler (128 or 256)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 8-bit swallow counter ($0 \leq A \leq 255$, $A < N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



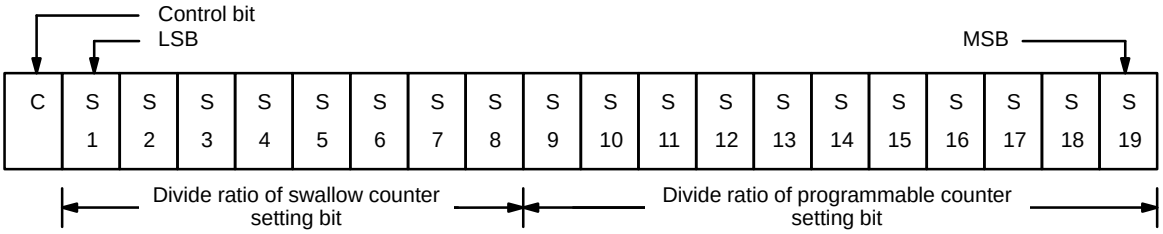
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 128/129
SW=L : 256/257
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 20-bit shift register, 19-bit latch, 8-bit swallow counter and 11-bit programmable counter. Serial 20-bit data format is shown below.



8-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S8	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•
255	1	1	1	1	1	1	1	1

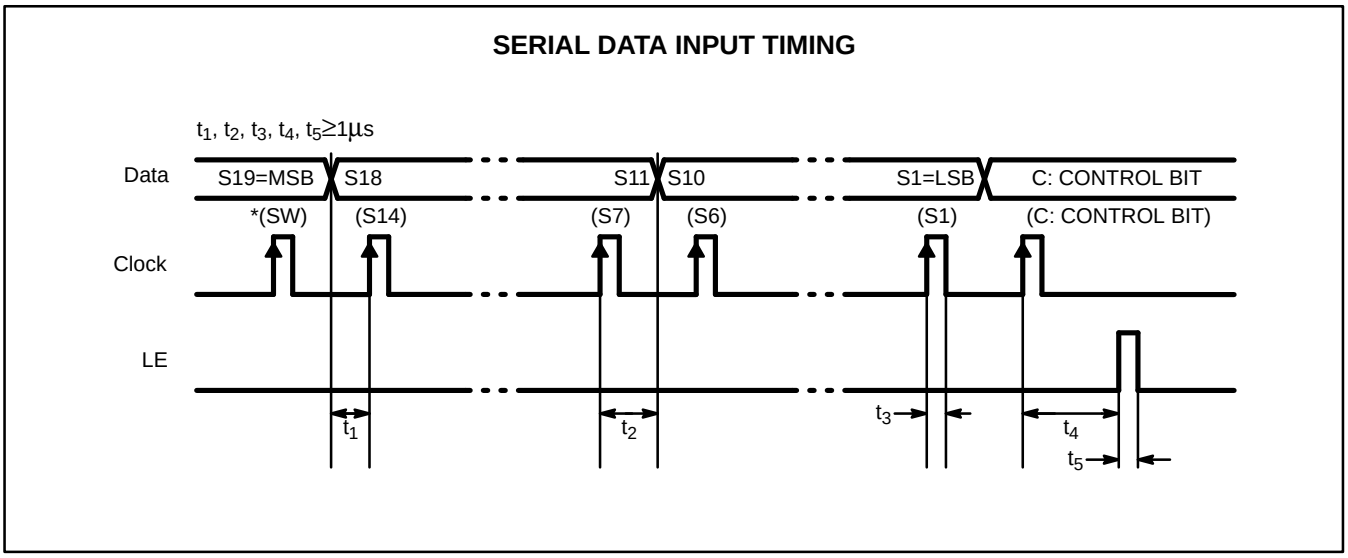
NOTE: Divide ratio: 0 to 255

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S8: Swallow counter divide ratio setting bit. (0 to 255)
S9 to S19: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets to low level).
Data is input from MSB side.

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data into the shift register.

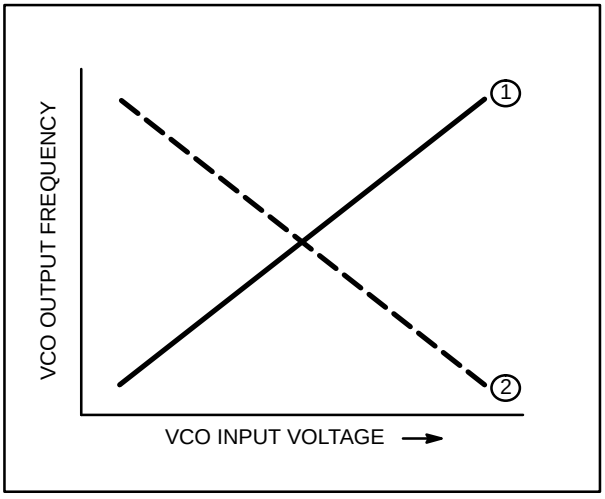
PHASE CHARACTERISTICS

FC pin is provided to change phase polarity of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (ØR, ØP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level.

	FC=H or open				FC=L			
	D_O	ØR	ØP	f_{out}	D_O	ØR	ØP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)

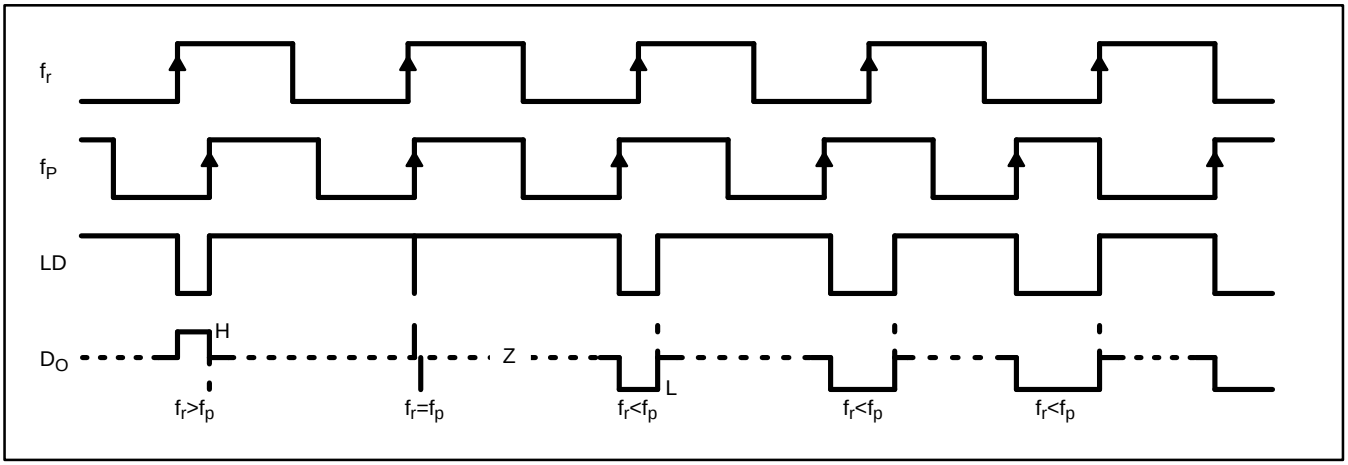
Note: Z=(High impedance)

VCO POLARITY



Depending upon VCO polarity, FC pin should be set accordingly:
When VCO polarity are like (1) , FC should be set High or open circuit;
When VCO polarity are like (2) , FC should be set Low.

PHASE DETECTOR OUTPUT WAVEFORM (FC=High)



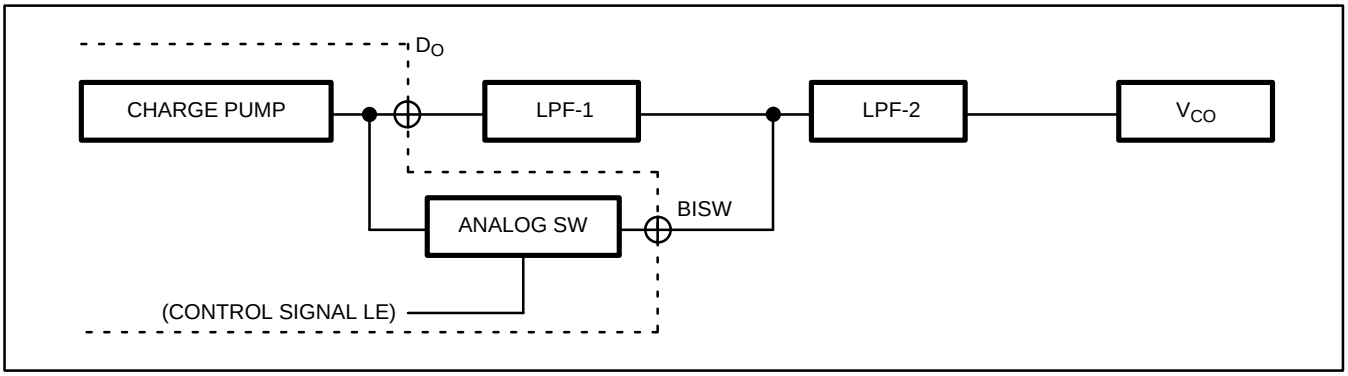
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) is connected to BISW pin. When the analog switch is OFF, BI-SW pin is set to high-impedance state.

LE	Analog Switch
H(Changing the divide ratio of internal prescaler)	ON
L(Normal operating mode)	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input Voltage	V_I	GND	—	V_{CC}	V
Operating Temperature	T_A	–40	—	85	°C

HANDLING PRECAUTIONS

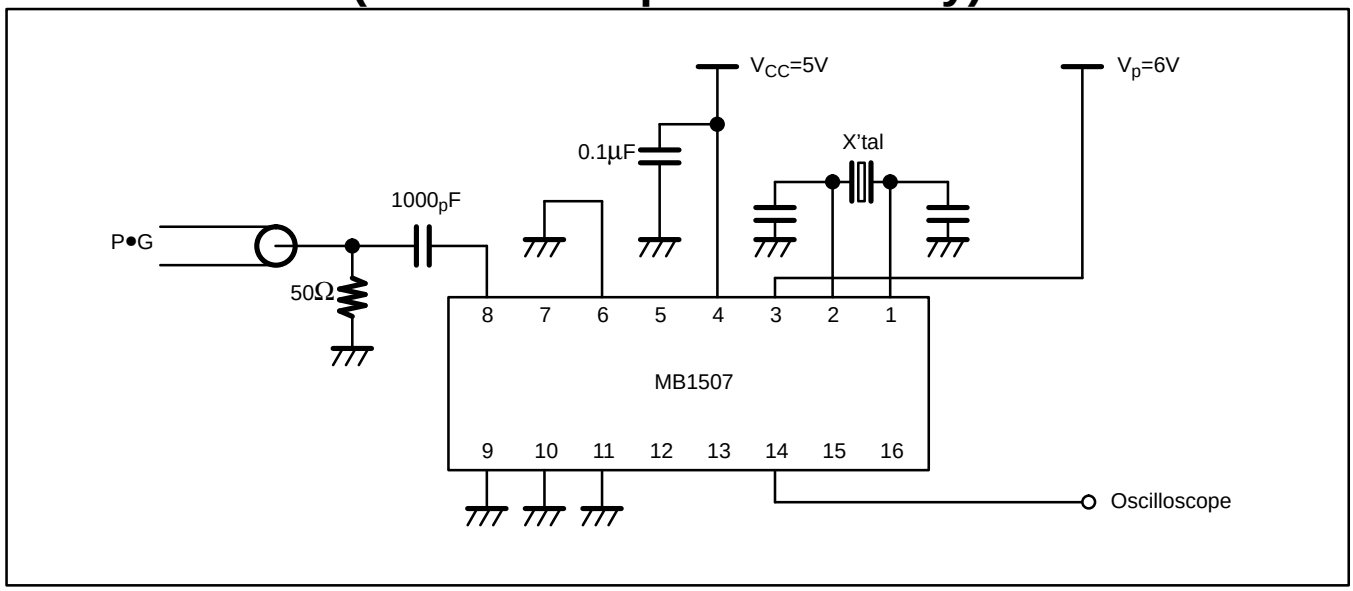
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

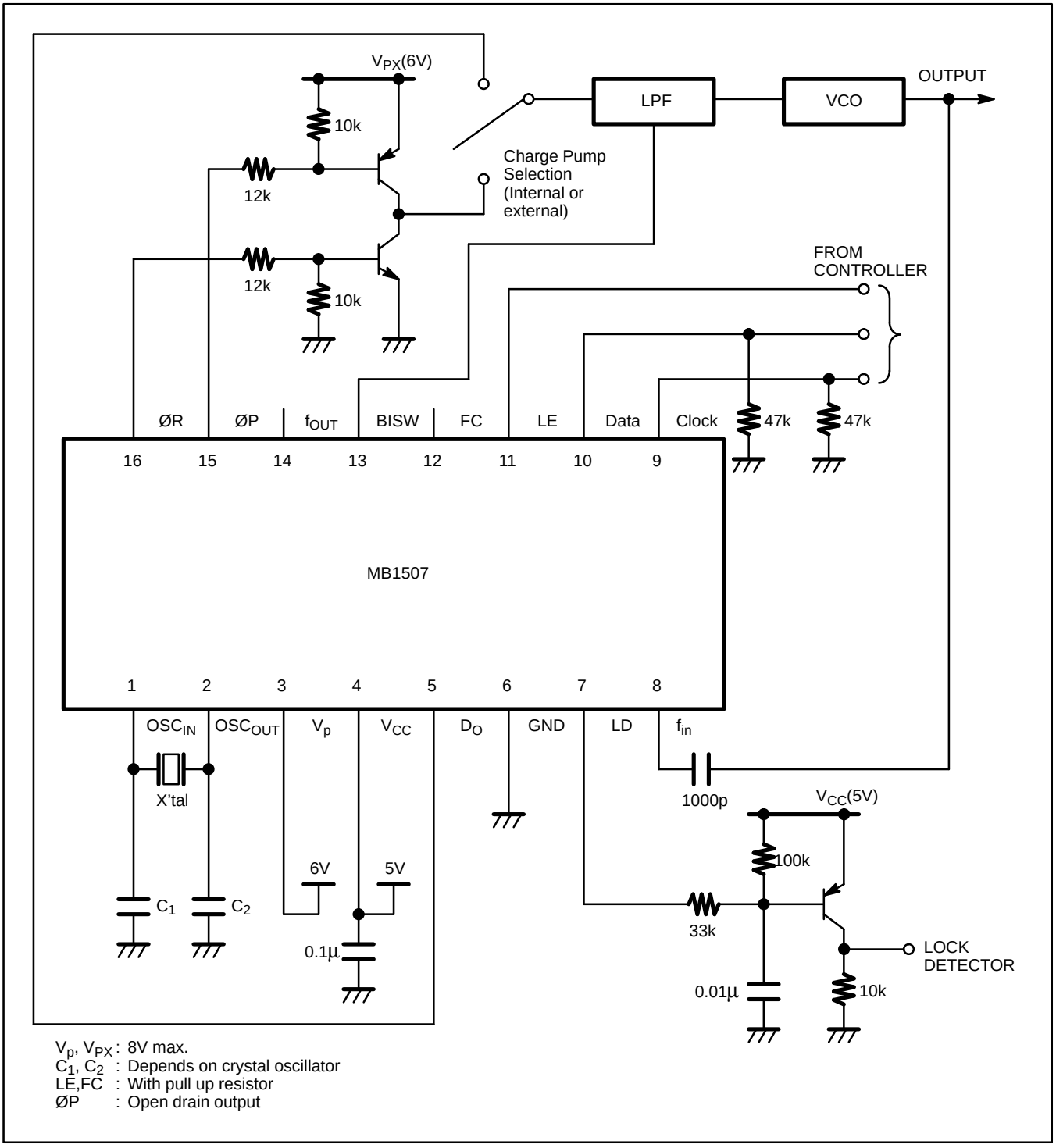
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1	—	18.0	—	mA
Operating Frequency	f_{in}	f_{in}	Note 2	10	—	2000	MHz
	OSC_{IN}	f_{OSC}	—	—	12	20	MHz
Input Sensitivity	f_{in}	P_{fin}	50Ω	–4	—	6	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	—	V_{CC}x0.7	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}	—	—	1.0	—	µA
Low-level Input Current		I_{IL}	—	—	–1.0	—	µA
Input Current	OSC_{IN}	I_{OSC}	—	—	±50	—	µA
	LE, FC	I_{LE}	—	—	–60	—	µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4	—	—	V
Low-level Output Current		V_{OL}		—	—	0.4	V
High Impedance Cutoff Current	D_O, ØP	I_{OFF}	V_P=V_{CC} to 8V V_{OOP}=GND to 8V	—	—	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}	—	–1.0	—	—	mA
		I_{OL}	—	1.0	—	—	mA
Analog Switch On Resistance		R_{ON}	—	—	25	—	Ω

NOTE 1: f_{in}=2.0GHz, f_{OSC} =12MHz X'tal V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured with a capacitor 1000$_P$F.

TEST CIRCUIT (Prescaler Input Sensitivity)



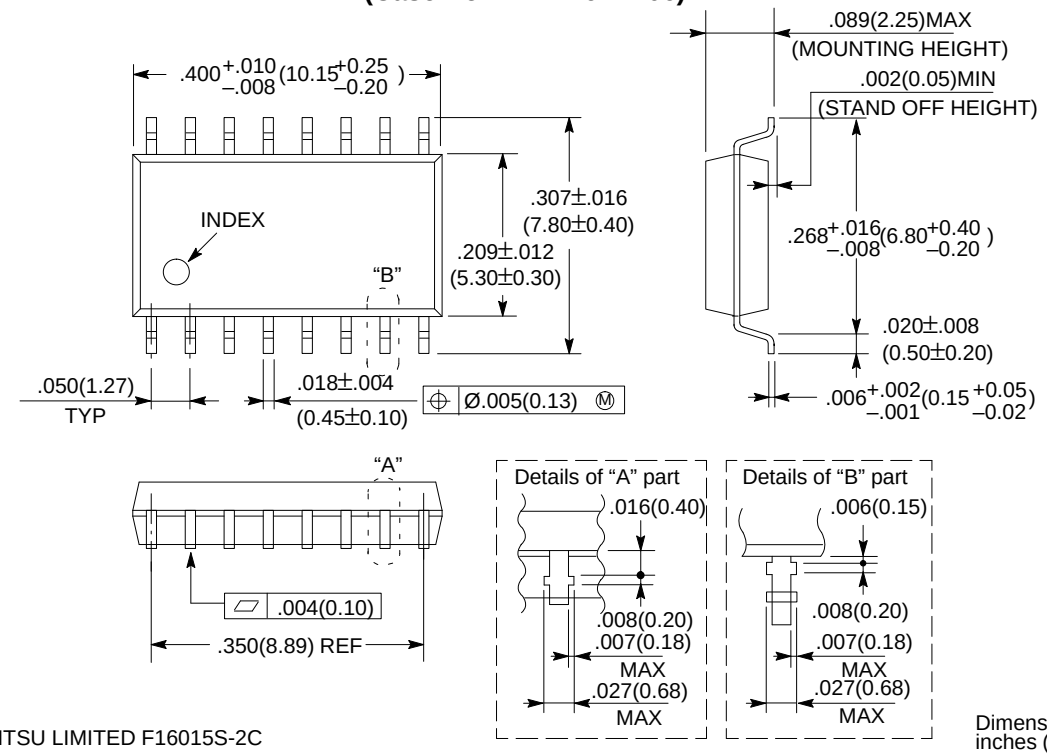
TYPICAL APPLICATION EXAMPLE



V_p, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-16P-M06)



Dimensions in inches (millimeters)

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