

### Features

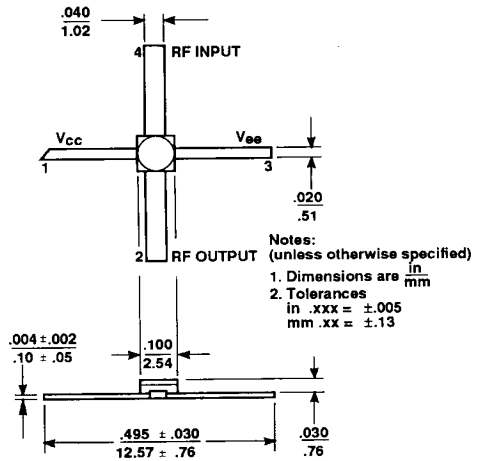
- **Wide Operating Frequency Range:**  
0.05 to 5 GHz typical
- **Low Phase Noise:** -140 dBc/Hz, 1 KHz offset
- **High Input Sensitivity:** -30 dBm at 1 GHz typical
- **Low Output Level:** -13 dBm typical
- **Single Supply Voltage:**  $V_{cc} = 5\text{ V}$
- **Low Power Dissipation:** 125 mW typical
- **Hermetic Gold-Ceramic Surface Mount Package**

### Description

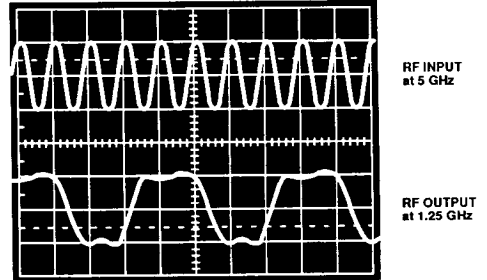
Avantek's IFD-50010 is a low-phase-noise silicon bipolar static digital frequency divider using two scaled Emitter-Coupled-Logic (ECL) master-slave D flip-flops and sensitive buffer amplifiers. It is housed in a hermetic, high reliability ceramic package suitable for commercial, industrial and military applications. Typical applications include stabilized or digitally controlled local oscillators for GPS, TVRO, DBS, cellular radio and military communications receivers, and frequency synthesizers and counters in instrumentation systems.

The IFD series of digital frequency dividers is fabricated using Avantek's 15 GHz  $f_T$ , 20 GHz  $f_{MAX}$  ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

### Avantek 100 mil Package



### Typical Output Response With 5 GHz Input



### Electrical Specifications<sup>1</sup>, $T_A = 25^\circ\text{C}$

Symbol	Parameters and Test Conditions: $V_{cc} - V_{ee} = 5\text{ V}$ , $Z_0 = 50\ \Omega$	Units	Min.	Typ.	Max.
F <sub>MAX</sub>	Maximum Clock Frequency $P_{in} = -10\text{ dBm}$ (200 mVpp)	GHz	4.5	5.0	
F <sub>MIN</sub>	Minimum Clock Frequency $P_{in} = -10\text{ dBm}$ (200 mVpp)	GHz		0.05	
IS	Input Sensitivity $f = 1\text{ GHz}$	dBm		-30	
		mVpp		20	
OL	Output Level $f = 0.05\text{ to }5\text{ GHz}$	dBm		-13	
		mVpp		140	
SL <sub>MAX</sub>	Highest Nonharmonic Spurious Level $f = 0.05\text{ to }5\text{ GHz}$	dBm		-35	
VSWR	Input VSWR $f = 0.05\text{ to }5\text{ GHz}$			1.5:1	
	Output VSWR $f = 0.05\text{ to }5\text{ GHz}$			2.0:1	
PN	SSB Phase Noise $f = 2\text{ GHz}$ , 1 kHz offset $f = 4\text{ GHz}$ , 1 kHz offset	dBc/Hz		-140	
				-135	
$T_r$	Output Rise Time $f = 5\text{ GHz}$	psec		100	
$T_f$	Output Fall Time $f = 5\text{ GHz}$	psec		100	
$I_{cc}$	Supply Current	mA	20	30	40

Note: 1. The recommended operating voltage range for this device is 4.5 to 5.5 V.

**Absolute Maximum Ratings**

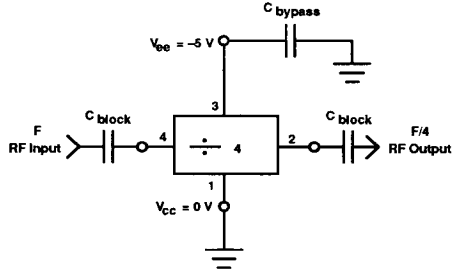
Parameter	Absolute Maximum <sup>1</sup>
Device Voltage	6 V
Power Dissipation <sup>2,3</sup>	250 mW
RF Input Power	+10 dBm
Junction Temperature	200°C
Storage Temperature	-65°C to 200°C

Thermal Resistance<sup>2,4</sup>:  $\theta_{jc} = 95^\circ\text{C/W}$

**Notes:**

1. Permanent damage may occur if any of these limits are exceeded.
2. TCASE = 25°C
3. Derate at 10.5 mW/°C for TC > 176°C
4. See MEASUREMENTS section "Thermal Resistance" for more information.

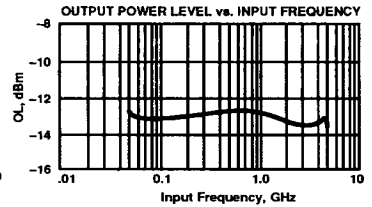
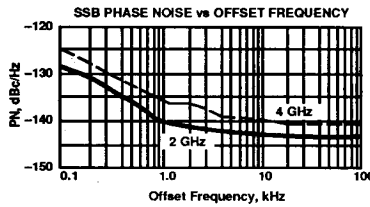
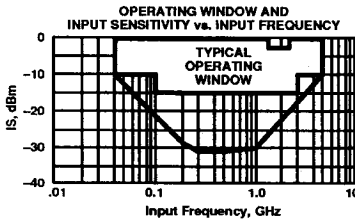
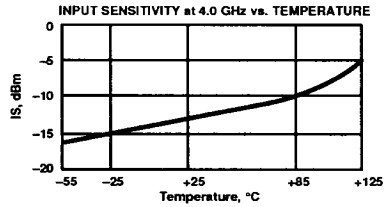
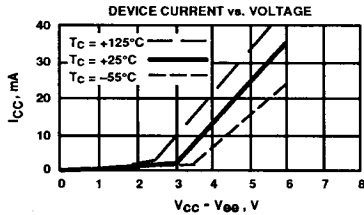
**Typical Biasing Configuration**



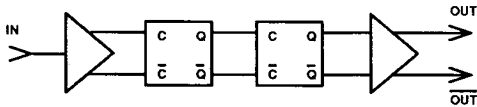
**Typical Performance, T<sub>A</sub> = 25°C**

P<sub>in</sub> = -10 dBm

(unless otherwise noted)



**Chip Block Diagram**



**Typical Stabilized LO Configuration**

